Abstract of the Disclosure:

A method and a configuration for generating a clock pulse in a data processing system having a number of independent, non-synchronous digital data channels, is described. A phase-locked loop (PLL) circuit derives a reference clock pulse, particularly from the data or a co-supplied clock pulse of a data channel serving as a reference channel, the acquired reference clock pulse is supplied to the data channels and a delay-locked loop (DLL) circuit compensates for differences in a clock pulse frequency between the reference clock pulse and the further data channels. As a result, only one reference clock pulse is sufficient in a data processing system having a number of independent, non-synchronous digital data channels, so that the jitter generated in the system is reduced.

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